LuLeey 800G OSFP SR8 Transceiver

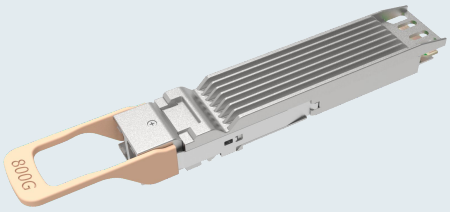
LuLeey 800G OSFP SR8 Transceiver is an 800Gb/s Octal Small Form-factor Pluggable optical module designed for 50m OM4/OM5 optical communication applications. On the transmitter side, the module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s. On the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data.

Product Features

- ✓ Compliant with OSFP MSA Hardware Type2 housing
- ✓ CMIS 5.0 compliance
- ✓ 800G SR8 multi-mode transceiver
- ✓ 53.125GBd PAM4 *8 channel 800GAUI-8 C2M Electrical interface
- ✓ 53.125GBd PAM4 *8 channel 800G-SR8 Optical interface
- ✓ 8 channels 850nm VCSEL array
- ✓ 8 channels PIN photo detector array
- ✓ Up to 50m reach on OM4/OM5 and 30m on OM3 with FEC
- ✓ Dual optical ports of MPO-12/APC
- ✓ Single 3.3V power supply
- ✓ Power dissipation <15W
- ✓ Case temperature range of 0 to 70°C

Applications

- ✓ 800GBASE-SR8 Ethernet
- ✓ InfiniBand



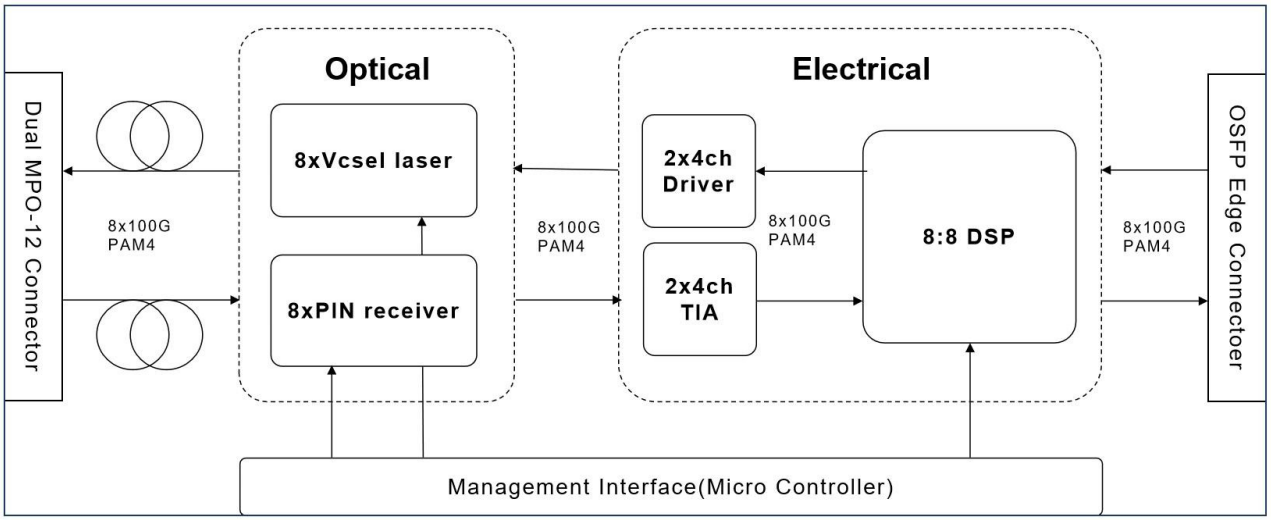
Product Selection

Part Number	Operating case temperature	DDMI	Package
LuLeey 800G OSFP SR8 Transceiver	Commercial (0~70℃)	Yes	OSFP Finned

Regulatory Compliance

- ESD compatible with MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM)
- Laser Eye Safety compatible with FDA 21CFR 1040.10 and EN (IEC) 60825-1
- RoHS compliance

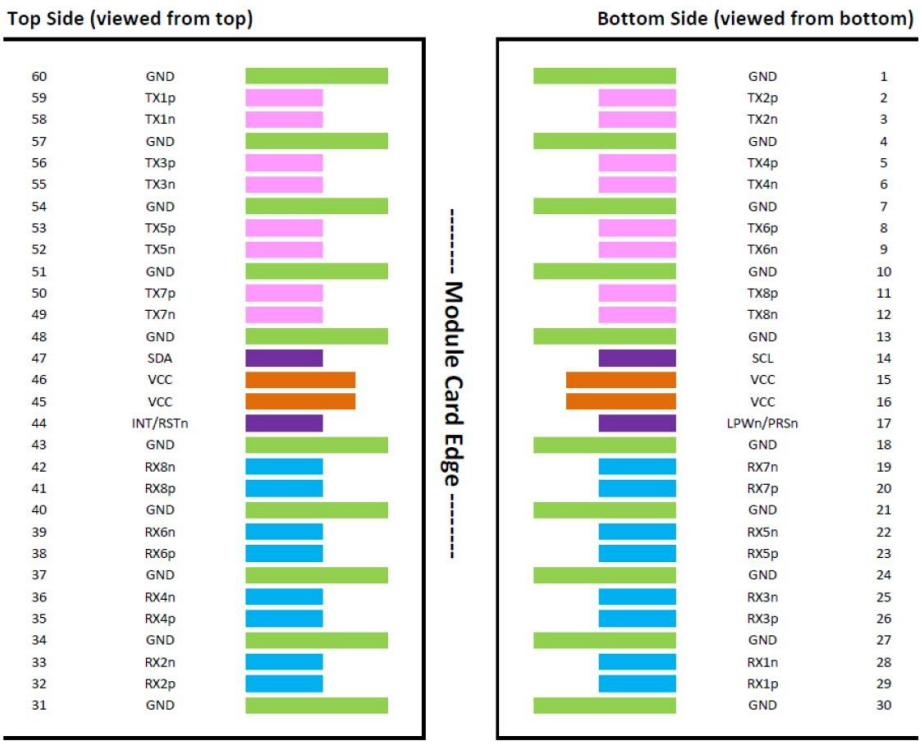
Transceiver Block Diagram



Pin Descriptions

Pin	Symbol	Description	Logic	Plug Sequence
1	GND		Ground	1
2	TX2p	Transmitter Data Non-Inverted	CML-I	3
3	TX2n	Transmitter Data Inverted	CML-I	3
4	GND		Ground	1
5	TX4p	Transmitter Data Non-Inverted	CML-I	3
6	TX4n	Transmitter Data Inverted	CML-I	3
7	GND		Ground	1
8	TX6p	Transmitter Data Non-Inverted	CML-I	3
9	TX6n	Transmitter Data Inverted	CML-I	3
10	GND		Ground	1
11	TX8p	Transmitter Data Non-Inverted	CML-I	3
12	TX8n	Transmitter Data Inverted	CML-I	3
13	GND		Ground	1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	3
15	VCC	+3.3V Power		2
16	VCC	+3.3V Power		2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	3
18	GND		Ground	1
19	RX7n	Receiver Data Inverted	CML-O	3
20	RX7p	Receiver Data Non-Inverted	CML-O	3
21	GND		Ground	1
22	RX5n	Receiver Data Inverted	CML-O	3
23	RX5p	Receiver Data Non-Inverted	CML-O	3
24	GND		Ground	1
25	RX3n	Receiver Data Inverted	CML-O	3

26	RX3p	Receiver Data Non-Inverted	CML-O	3
27	GND		Ground	1
28	RX1n	Receiver Data Inverted	CML-O	3
29	RX1p	Receiver Data Non-Inverted	CML-O	3
30	GND		Ground	1
31	GND		Ground	1
32	RX2p	Receiver Data Non-Inverted	CML-O	3
33	RX2n	Receiver Data Inverted	CML-O	3
34	GND		Ground	1
35	RX4p	Receiver Data Non-Inverted	CML-O	3
36	RX4n	Receiver Data Inverted	CML-O	3
37	GND		Ground	1
38	RX6p	Receiver Data Non-Inverted	CML-O	3
39	RX6n	Receiver Data Inverted	CML-O	3
40	GND		Ground	1
41	RX8p	Receiver Data Non-Inverted	CML-O	3
42	RX8n	Receiver Data Inverted	CML-O	3
43	GND		Ground	1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	3
45	VCC	+3.3V Power		2
46	VCC	+3.3V Power		2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	3
48	GND		Ground	1
49	TX7n	Transmitter Data Inverted	CML-I	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	3
51	GND		Ground	1
52	TX5n	Transmitter Data Inverted	CML-I	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	3
54	GND		Ground	1
55	TX3n	Transmitter Data Inverted	CML-I	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	3
57	GND		Ground	1
58	TX1n	Transmitter Data Inverted	CML-I	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	3
60	GND		Ground	1



Pin-out of Connector Block on Host Board

OSFP Control Pins

Parameter	Function	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Input/output	Dual Function Signal • Low Power mode is an active-low input signal • Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal
INT/RSTn	Input/output	Dual Function Signal • Reset is an active-low input signal • Interrupt is an active-high output signal

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Storage Temperature	Tstg	-40		+85	°C	
Maximum Supply Voltage	VCC	-0.5		3.5	V	
Operating Relative Humidity	RH	0		85	%	Non-condensing

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Case Operating Temperature	Tc	0		+70	°C	
Power Supply Voltage	Vcc	3.135	3.3	+3.465	V	
Power Consumption				15	W	
Maximum Power Dissipation, Low Power Mode				1.5	W	
Data Rate, each Lane			53.125		GBd	PAM4
Two Wire Serial Interface Clock Rate		100		1000	kHz	
Power Supply Noise Tolerance (10Hz - 10MHz)		66			mV	
Rx Differential Data Output Load			100		ohm	
Link Distance (OM4/OM5)				50	m	
Link Distance (OM3)				30	m	

Electrical Characteristics

Parameter	Test Point	Min	Typ	Max	Unit	Notes
Module input (each Lane)						
Signaling Rate, each lane	TP1		53.125±100ppm		GBd	
DC common-mode voltage tolerance	TP1	-350		2850	mV	
Single-ended voltage tolerance range	TP1a	-0.4		3.3	V	
AC Common-Mode Voltage Tolerance Low-Frequency, VCMLF Full-Band, VCMLF	TP1a	 32 80			 mV	
Module stressed input tolerance	TP1a	IEEE 802.3ck D3.3 120G.3.4.3				
Differential Voltage pk-pk Tolerance	TP1a	750			mV	
Differential-mode to common-mode return loss, RLcd	TP1	IEEE 802.3ck D3.3 Equation 120G-2			dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	
Module output (each Lane)						
Signaling Rate, each lane	TP4		53.125±100ppm		GBd	
Peak-to-peak AC common- mode voltage Low-frequency, VCMLF Full-band, VCMFB	TP4			 32 80	 mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	 mV	
Eye Height	TP4	15			mV	
Vertical Eye Closure, VEC	TP4			12	dB	
Common-Mode to Differential Return Loss, Rldc	TP4	IEEE 802.3ck Equation 120G-1			dB	

Effective return loss, ERL	TP4	8.5		dB	
Differential termination mismatch	TP4		10	%	
Transition time (20% to 80%)	TP4	8.5		ps	
DC common-mode output voltage	TP4	-350	2850	mV	

Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Data Rate, each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Center Wavelength	λc	844	850	863	nm	
RMS spectral width				0.6	nm	
Average Launch Power, each Lane	PAVG	-1		4	dBm	1
Outer Optical Modulation Amplitude, each Lane max (OMAouter), each Lane	POMA	-2.1		3.5	dBm	2
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.4	dB	
Average launch power of OFF transmitter	Toff			-30	dBm	
Extinction Ratio	ER	2.5		3.5	dB	
$RIN_{14}OMA$	RIN		-148		dB/Hz	
Optical Return Loss Tolerance	ORLT			14	dB	
Transmitter Reflectance	TR			-26	dB	3
Receiver						
Data Rate, each Lane			53.125 ± 100 ppm		GBd	
Modulation Format			PAM4			
Center wavelength	λc	842	850	863	nm	
Damage Threshold, each Lane		5			dBm	
Average Receive Power, each Lane		-6.3		4	dBm	
Receive Power (OMAouter), each Lane				3.5	dBm	
Receiver Reflectance				-20	dB	
Receiver Sensitivity (OMAouter), each Lane				-4.6	dBm	4
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-2	dBm	5
LOS Assert	LOSA	-17			dBm	
LOS De-assert	LOSD			-8	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.4		dB	
OMAouter of each aggressor lane			3.5		dB	

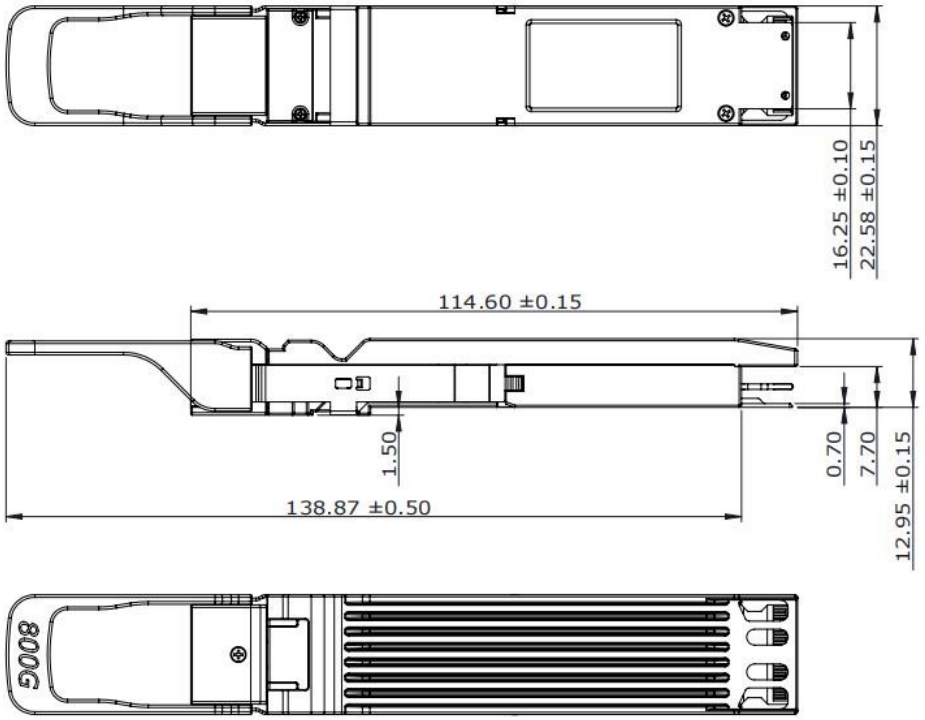
Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Even if max(TECQ,TDECQ) < 1.8dB, OMAouter (min) must exceed this value.
3. Transmitter reflectance is defined looking into the transmitter.

4. Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with TDECQ<=1.8dB

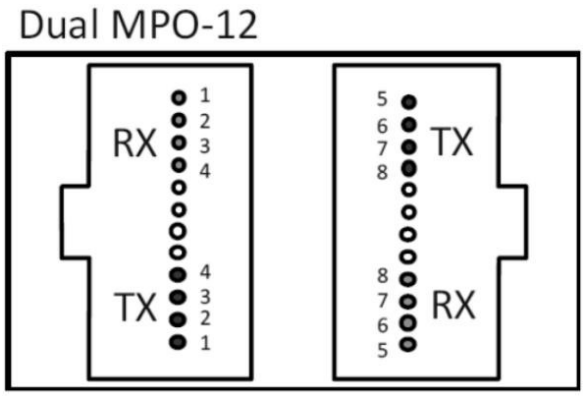
5. Measured with conformance test signal at TP3 for the BER equal to $2.4x10^{-4}$.

Mechanical Specifications



Optical Port Description

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in following figure when looking into the MDI receptacle with the connector key way feature on top.



Digital Diagnostic Monitoring Interface

Five transceiver parameter values are monitored. The following table defines the Monitory parameter's accuracy.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3		3	°C	
Supply voltage monitor absolute error	DMI_VCC	-3		3	%	
Bias current monitor absolute error	DMI_I Bias	-10		10	%	
Tx power monitor absolute error	DMI_TX	-3		3	dB	
Rx power monitor absolute error	DMI_RX	-3		3	dB	